Notice of Allowability	Application No.	Applicant(s)	
	10/688,139	SCHIFF, TOD F.	
	Examiner	Art Unit	
	Y. J. Han	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *an IDS filed on 10/16/03*.

2. ☒ The allowed claim(s) is/are *1-21*.

3. ☒ The drawings filed on *16 October 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 10/16/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

JESSICA HAN
PRIMARY EXAMINER

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-21 are allowed.

2. The following is an examiner's statement of reasons for allowance:

Claim 1 recites, inter alia, a control circuit which provides said N control signals to said N phases during a switching cycle which has a period T and a frequency f1, said control signals phase-shifted by T/N with respect to each other such that said phases are synchronously switched in a prescribed sequence, said phases providing respective phase currents which are summed together; and at least one additional phase, each of said additional phases comprising a current generating circuit which provides a current I_{hp} in response to a control signal, said current I_{hp} having a switching frequency f2 which is equal to or greater than f1, said current I_{hp} summed with said N phase currents to provide an output current Iout to a load connected to said output terminal, said current I_{hp} providing energy which improves the converter's response to load changes.

Claim 9 recites, inter alia, a control circuit which provides said N control signals to said N phases during a switching cycle which has a period T and a frequency f1, said control signals phase-shifted by T/N with respect to each other such that said phases are synchronously switched in a prescribed sequence, said phases providing respective phase currents which are summed together; and at least one additional phase, each of said additional phases comprising: a logic gate which receives said N control signals at respective inputs and combines them into a single control signal which has a switching frequency equal to N*f, a driver connected to receive said single control signal and to toggle an output when any of said N control signals are provided to

their respective phases, an output inductor connected between said output terminal and a common node, and a switching circuit connected to said common node and arranged to conduct current to and from said output inductor in response to said driver output to provide a current I_{hp} having a switching frequency equal to N*f, said current I_{hp} summed with said N phase current to provide an output current Iout to a load connected to said output terminal, said current I_{hp} providing energy which improves the converter's response to load changes.

Claim 13 recites, inter alia, a control circuit which provides said N control signals to said N phases during a switching cycle which has a period T and a frequency f1, said control signals phase-shifted by T/N with respect to each other such that said phases are synchronously switched in a prescribed sequence, said phases providing respective phase currents which are summed together to provide an output current Iout to a load connected to said output terminal, the duty cycles of said N PWM control signals varying with said load, and at least one additional phase arranged to reduce Iout by a current I_{hp} when the duty cycles of all of said control signals are approximately zero due to a load release, to reduce Vout overshoot that might otherwise occur in response to said load release.

Claim 19 recites, inter alia, a control circuit which provides said N control signals to said N phases during a switching cycle which has a period T and a frequency f1, said control signals phase-shifted by T/N with respect to each other such that said phases are synchronously switched in a prescribed sequence, said phases providing respective phase currents which are summed together to provide an output current Iout to a load connected to said output terminal, the duty cycles of said N PWM control signals varying with said load, said control circuit further providing a clock signal Fclk which is pulsed at the start of each of said N control signals'

switching periods such that Fclk has a frequency N*f, and at least one additional phase arranged to reduce Iout by a current I_{hp} when the duty cycles of all of said control signals are approximately zero due to a load release, to reduce Vout overshoot that might otherwise occur in response to said load release, each of said additional phases comprising: a logic gate which receives said N control signals and combines them into a single control signal Fpwm which has a switching frequency equal to N*f when the duty cycles of said N control signals is non-zero, a reset-dominate flip-flop connected to receive said control signal Fpwm at its reset input and said clock signal Fclk at its set input such that said flip-flop's output is reset whenever a non-zero Fpwm control signal is received and is set whenever Fpwm is zero when Fclk is received, and an output current reduction circuit coupled to said flip-flop output and arranged to conduct said current I_{hp} when said flip-flop output is set.

The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include either of the above limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Y. J. Han whose telephone number is 571-272-2078. The examiner can normally be reached on Mon-Fri 5:30am-2:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J. Han
Primary Examiner
Art Unit 2838